ISSN:0975-9646

QPSK Modulator on FPGA using 64 Values ROM

Prashant D. Thombare, Ameed. M. Shah

Government College of Engineering,
Kathora Naka Road, Amravati, India

***Abstract*— In many applications such as TDMA cellular telephone, OFDM, Bluetooth, Satellite communication etc. QPSK digital modulation technique is used due to its higher bandwidth efficiency, higher noise immunity and simpler circuit. Simpler circuit is having lower cost, smaller size and lower power dissipation. In this paper a new circuit for QPSK modulator is designed which improves the area of the circuit. It is having lower logic elements than conventional design which provide same output. The circuit designing is performed on Active-HDL9.2 and implemented on Spartan II (XC2S30-5PQ208) FPGA board using Xilinx ISE9.1i and results are observed on DSO using Digital to Analog Convertor (DAC). The area of the design is found to be lower in total logic elements than the conventional design.**

***Keywords*— QPSK, FPGA, ROM, Flip-Flops, Modulation etc.**

I. INTRODUCTION

Modulation is the process of combining data signal with carrier signal to transmit it to the receiver for protection of the data signal from atmospheric noise or fading effect. There are two types of modulation techniques i.e., analog and digital. In analog modulation technique carrier signal is modulated with the help of analog data signal such as AM, FM, PM etc. and in digital modulation technique carrier signal is modulated with the help of digital data signal it is also called as keying technique e.g. ASK, FSK, PSK. Change in phase of carrier signal is called phase shift keying such as BPSK, QPSK, 8-PSK, 16-PSK etc. in general M-ary PSK where M is no. of phase shifts in the carrier signal. In QPSK, two signals can be modulated at a time. Its BER is lower than higher order PSKs such as 8-PSK, 16-PSK etc which are easily affected by noise. Higher order PSKs consume more power and having complex circuitry as compared to QPSK. QPSK is having moderate data transfer speed, more bandwidth efficiency as well as power efficiency.

There are many applications where QPSK modulator is used, out of which few are of battery operated devices such as Bluetooth, TDMA cellular communication, Medical Implant Communication Services (MICS) etc. therefore it is necessary to minimize the area and power consumption of these devices. Digital devices are becoming smaller in size, hence considering this issue the lower size modulator is designed, which provides same output as conventional modulator.

II. CONVENTIONAL MODULATOR

A. The model of QPSK

The QPSK modulator can modulate two signals in same frequency band. Each signal is to be converted from analog to digital, this digital signal is encoded by encoder then modulation is takes place. One signal is modulated with sine and another with cosine which gives four (two of each) different phases, by adding these two phase shifted signals we get QPSK output signal [1].

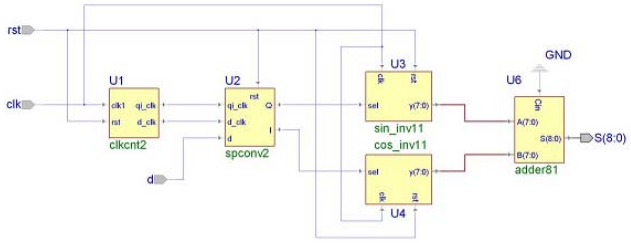

Fig. 1 Conventional QPSK Modulator with two ROMs

The above figure shows the block diag. of conventional QPSK modulator in which spconv2 (serial to parallel converter) block takes data (d) as input and separate it into two signals Q and I. There are two BPSK blocks, sin_inv11 and cos_inv11. Each block is consists of a ROM, Subtracter and MUX which generate BPSK output waveform. ROM block give sine wave, subtracter give inverse sine wave and MUX block select each one according to sel input i.e. for sel as '0', sin block produce sine wave and for '1' it gives invert sine wave similarly for cos block. These four combinations of two inputs are added into adder block to produce QPSK as output waveform. It consists of total 9 bits (8 bits data and 1 bit carry). Carry bit is generated due to addition of two 8 bits data signal.

B. Mathematical equation of QPSK Modulator

The QPSK signal can be given as

$$S_{QPSK} = \sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + (2i -1) \pi/4) \quad (1)$$

for i = 1, 2, 3, 4

Where,

$\sqrt{\frac{2Es}{Ts}}$ = Constant amplitude with *Es* energy and *Ts* time period of the signal

f_c= Frequency of carrier signal
i = phase no. of signal as per the symbols of the data signal from the trigonometric equation given below,

$$\cos(A+B) = \cos(A)\cos(B) - \sin(A)\sin(B) \quad (2)$$

from eq. (2) we can write,

$$S_{QPSK}= \sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t)\cos[(2i-1)\pi/4]- \sqrt{\frac{2Es}{Ts}} \sin(2\pi f_c t)\sin[(2i -1)\pi/4] \quad (3)$$

Fig.1. Shows that separate sine and cosine waves are generated which require two ROM's to store these signals [2]. They are then modulated by the input binary data signal. These two signals are then added to generate the QPSK signal. All these process is discuss in [5] with design flow diagram.

There are two signals in QPSK signal i.e. in-phase I(t) and Quadrature phase Q(t). Which is given in eq. (3) can be written as

$$S_{QPSK} = \sqrt{\frac{2}{Ts}} \cos(2\pi fct)I(t) - \sqrt{\frac{2}{Ts}} \sin(2\pi fct)Q(t)$$

where,
$I(t) = \sqrt{Es} \cos[(2i -1)\pi/4]$ and
$Q(t) = \sqrt{Es} \sin[(2i -1)\pi/4]$

Output QPSK waveform with four different phase shifts is as shown in figure 2. In this, we can see that for each symbol phase angle of original signal is different.

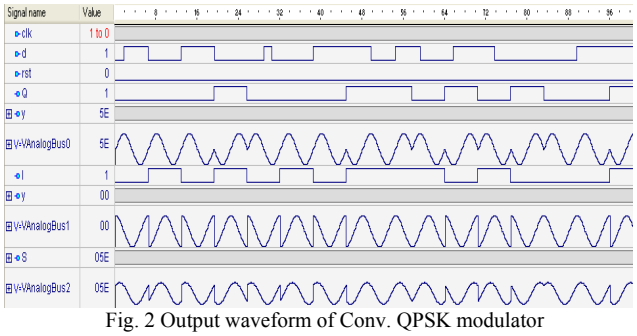

Fig. 2 Output waveform of Conv. QPSK modulator

III. Proposed Work

We know that, day by day electronic devices are getting smaller in size also reduction in its cost. It means the area is one of the main factors while designing digital circuit. The required amount of components for any circuit should be as less as possible which produce same output.

While designing any circuit all the other factors such as power dissipation, capacitance, clock timing etc. needs to consider and assure that all these factors are in certain limit. In this paper main focus is given on reducing the actual size of conventional QPSK Modulator by reducing the no. of logic elements in the design.

From eq. (1) we can say that S_{QPSK} is having only cos term, it means output waveform is consist of only cosine wave with different phase shifts according to variable 'i'. Considering this factor, a ROM is developed which will generate only cosine wave with different values of 'i' taken as symbol or combination of Q and I i.e. 4 values.

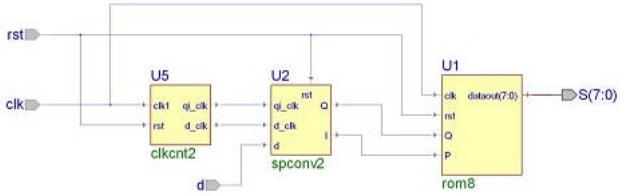

Fig. 3 Proposed QPSK Modulator with one ROM

As shown in fig above the sin_inv11, cos_inv11 and adder are replaced by single block i.e. rom8. It takes Q and I as two input signals. According to change in input there will be change in phase of signal. Rom8 block is having 64 different values of a sin wave. The particular symbol (combination of Q and I) starts the waveform from particular value for that phase. After that, sine wave continues until there is change in symbol. In this case there is no addition of two waves hence the output is of 8 bits and there is no carry.

TABLE I
PHASE SHIFTED SIGNAL FOR DIFFERENT INPUT SYMBOLS

Symbol	Bits	S(t)	Phase (Deg.)	Mod. Signal
S1	00	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{5\pi}{4})$	225^0	
S2	01	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{3\pi}{4})$	135^0	
S3	10	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{7\pi}{4})$	315^0	
S4	11	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{\pi}{4})$	45^0	

Above table shows that, the phase change of the signal is depend on the change in symbols, each symbol is having particular phase angle or signal pattern. In ROM these phases are achieved by selecting different symbols and starting the wave from particular value.

The output waveform of proposed blocks, which is as shown below which is similar to the conventional modulator waveform. It shows same phases for each symbol.

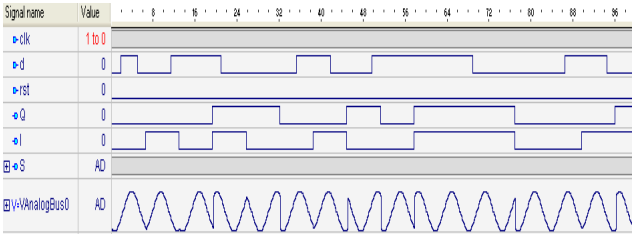

Fig. 4 Output waveform of Proposed QPSK modulator

IV. RESULTS

There are total four different designs, two for 16 values and two for 64 values ROM of conv. and proposed architecture are discussed in this paper and their device utilization are as shown below.

TABLE II
COMPARISON BETWEEN DIFFERENT DESIGNS

Logic utilization	16 values ROMs		64 values ROMs	
	Conv. Design (A)	Proposed Design (B)	Conv. Design (C)	Proposed Design (D)
No. of slice flip flops	117	75	131	75
No. of 4 i/p LUTs	220	141	309	210
No. of occupied slices	203	97	255	131
No. of slices containing only related logic	203	97	255	131
Total no. of 4 i/p LUTs	381	178	470	247
No. used as logic	220	141	309	210
No. used as route-through	161	37	161	37
No. of bonded IOBs	12	11	12	11
Total equivalent gate count	3,380	1,954	4,068	2,400

From results, we can see that design B is having lowest logic elements as compared to others. Design D shows large difference between all the parameters than design C and also design A. From this we can say that design D is better in area utilization than design C and A, while the design B is best among all. In this way the smaller size of QPSK modulator has achieved in proposed architectures.

Design C and D is having total 64 values in their ROMs which take 64 clock pulses to read the one waveform data (data to produce one wave) whereas design A and B is having 16 ROM values and require 16 clock pulses. The speed of the design is depends on clock timing and the clock timing is depend on physical parameters in the circuit such as capacitance, inductance, loading resistance etc. All these parameters are affected by the area of the design. From this we can say that the speed of operation is depends on the size or area of the design. The comparison of clock timing (ns) of all the designs is as shown below.

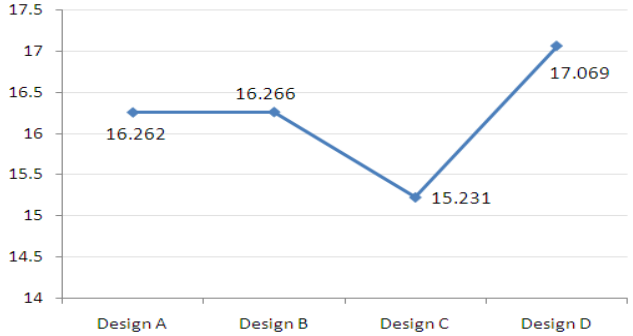

Fig. 5 Clock timing of different designs in ns

From figure 5, design C takes 1.035ns less time than design B, since it is having larger size than design B. Conventional designs are taking somewhat lesser time than proposed one but it is having larger size.

The comparison of power dissipation of all the designs is as shown below

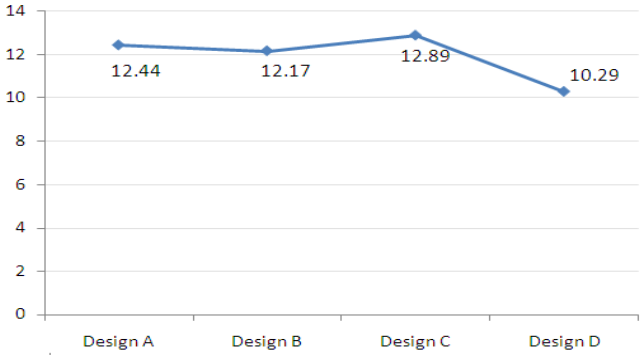

Fig. 6 Power dissipation of different designs

In above figure, design D is having lowest power dissipation while it is having highest clock timing, as power dissipation depends on it, higher the clock timing lower is the speed of operation and lower the power dissipation.

V. CONCLUSION

In this paper the design is proposed on Spartan-II (XC2S30-5PQ208) FPGA kit and observed that with change in no. of blocks and logical coding, actual size i.e. no. of logic elements of the circuit changes. In this paper, we get the smaller size QPSK modulator which gives same output as the conventional modulator by making some changes in no. of blocks and logical coding.

There are two types of designs developed in this paper i.e. 16 values (designs A and B) and 64 values (designs C and D) ROMs. ROMs in designs C and D take more size to store data and making circuit for it than designs A and B resp. Larger the size of ROM, sharper will be the waveform and gives fine phase shifts which help to detect easily at the receiver. But it takes higher logic elements at transmitter.

The new design is developed by replacing some blocks (sin_inv11, cos_inv11 and adder etc.) by the only one ROM block containing different ROM values for a wave, the phase shifting is achieved by taking Q and I as input and starting the wave from particular value for particular symbol.

From the results of clock timing we can conclude that larger size of the circuit take lesser time or having higher speed than smaller size devices. The power dissipation is inversely proportional to the speed of operation. Design D is having lowest power dissipation also it is having smaller size than design A; hence this design is developed despite design B is having smallest size. Designs B, C and D are best in area, speed and power dissipation resp. accordingly different designs are used in different applications.

ACKNOWLEDGMENT

We acknowledge to all the teaching, non teaching staff of our institute who has help us to fulfillment of this project work, also the colleagues who provide us all the required tools for this project.

REFERENCES

[1] S.O. Popescu, A.S.Gontean and D.Ianchis, "QPSK Modulator on FPGA," *IEEE 9th International Symposium on Intelligent Systems and Informatics,* September 8-10, 2011, Subotica, Serbia

[2] Wenmiao Song, Qiongqiong Yao, "Design and Implement of QPSK Modem Based on FPGA".

[3] Michal Kováč "BPSK, QPSK Modulator Simulation Model"

[4] A. Amsavalli, K.R. Kashwan, "FPGA Implementation of Low Complexity VLSI Architecture for DS-CDMA Communication System," *International Journal of Computer Applications* (0975 – 8887) Volume 42– No.20, March 2012

[5] K. A. Monpara, S. B. Parmar, "Design and Implementation of QPSK Modulator Using Digital Subcarrier," *Journal of Information, Knowledge and Research in Electronics and Communication Engineering*, ISSN: 0975 – 6779, Nov 11 to Oct 12, Volume – 02, Issue - 01 p.no. 394-398

[6] G. Elamary, G. Chester, J. Neasham, "A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGA for Biomedical Devices Applications," *Proceedings of the World Congress on Engineering* 2009 Vol. I, WCE 2009, July 1 - 3, 2009, London, U.K.

[7] A. M. Moubark, Mohd. Alauddin Mohd. Ali, Sawal Hamid Md Ali, Hilmi Sanusi, "FPGA Implementation of Low Power Digital QPSK Modulator using Verilog HDL," *Journal of Applied Science* 13(3): 385-392, 2013

[8] A.M.Bhavikatti, Subhash Kulkarni, Uday Kalyani, " FPGA Implementation of π/4 -QPSK Modulator and Demodulator," *IJCEM International Journal of Computational Engineering & Management,* Vol. 15 Issue 4, July 2012

[9] T. Sakla, D. Jain, S. Gautam, "Implementation of Digital QPSK Modulator By Using VHDL /Matlab," *International Journal of Engineering Science and Technology,* Vol. 2(9), 2010, pp.4827-4831

[10] B. Krongold, Timo Pfau, N. Kaneda and S. C. Jeffrey Lee, "Comparison Between PS-QPSK and PDM-QPSK With Equal Rate and Bandwidth," *IEEE Photonics Technology Letters,* Vol. 24, No. 3,pp. 203-205 Feb. 1, 2012

[11] Jason H. Anderson, F. N. Najm, and Tim Tuan, "*Active Leakage Power Optimization for FPGAs*," pp. 33-41

[12] Zhongxia He, Jingjing chen, "A Novel FPGA-based 2.5 Gbps D-QPSK Modem for High Capacity Microwave Radios".

[13] V. G. Mangale, U. L. Bombale, "BPSK Transmitter design using FPGA with DAC and pulse Shaping filter to minimize Inter-Symbol Interference(ISI)," *IOSR Journal of Computer Engineering, ISSN:2278-0661, pp:30-33*